REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed July 14, 2008. Upon entry of this response, claims 1 – 20 remain pending. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Claims 14 – 20 are Allowable

As an initial matter, the Office Action appears to neglect addressing claims 14 – 20. Accordingly Applicants respectfully submit that the present Office Action is deficient pursuant to 37 C.F.R. 1.104(b), which states "[t]he examiner's action shall be complete as to all matters..." Applicants respectfully submit that claims 14 – 20 are allowable and requests indication of allowance. Alternatively, if claims 14 – 20 are rejected in a subsequent Office Action, any such Office Action must be non-final.

II. Objections to the Drawings

The Office Action indicates that the drawings are objected to as failing to comply with 37 CFR 1.121(d) because one or more of the drawings are allegedly illegible. Applicants amend the drawings, to correct the allegedly illegible portions, as indicated above.

III. Rejections Under 35 U.S.C. §103

A. Claim 1 is Allowable Over *Priem* in view of *Gaytan*

The Office Action indicates that claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Number 6,282,587 ("*Priem*") in view of U.S. Patent Number 5,638,367 ("*Gaytan*"). Applicants respectfully traverse this rejection for at least the reason that *Priem* in view of *Gaytan* fails to disclose, teach, or suggest all of the elements of claim 1. More specifically, claim 1 recites:

> A method for transferring network packet data stored in memory to an output device, the method comprising the steps of:
> concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet ***to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word***;
> storing the first sequence of packet data octets in a FIFO buffer operably connected to the output device ***when the octet length of the sequence of packet data octets is equal to the octet length of a data word***; and
> storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence ***in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.***
> ***(Emphasis added).***

Applicants respectfully submit that claim 1 is allowable over the cited art for at least the reason that neither *Priem* nor *Gaytan*, taken alone or in combination, discloses, teaches, or suggests a "method for transferring network packet data stored in memory to an output device, the method comprising the steps of… concatenating one or more packet data octets… ***to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word***… storing the first sequence of packet data octets in a FIFO buffer… ***when the octet length of the sequence of packet data octets is equal to the octet length of a data word***… [and] storing a first subset of packet data octets… in the FIFO buffer

and storing a remaining second subset of packet data octets from the first sequence ***in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word...*** " as recited in claim 1.

First, the Office Action argues that *Gaytan* discloses "concatenating the first sequence..." (OA page 4, line 13). Applicants respectfully disagree. More specifically, *Gaytan* discloses "perform[ing] packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry; namely, a word packing circuit and a byte packing circuit. Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 54). As illustrated in this passage, *Gaytan* appears to disclose packing operations but fails to disclose anything related to "concatenating one or more packet data octets... ***to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word***" as recited in claim 1.

Second, the Office Action argues that *Gaytan* discloses "storing a first sequence of packet data octets when the octet length of the sequence of data" (OA page 4, line 17). Applicants respectfully disagree. More specifically, *Gaytan* discloses "perform[ing] packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry; namely, a word packing circuit and a byte packing circuit. Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 54). As illustrated in this passage, *Gaytan* appears to disclose always storing data in the TX buffer. Consequently, *Gaytan* fails to even suggest "storing the first sequence of packet data octets in a FIFO buffer... ***when the octet length of the sequence of packet data octets is equal to the octet length of a data word***" as recited in claim 1. Further, *Gaytan* does not even appear to suggest making a determination of octet length, as implicitly recited in this element of claim 1.

Third, the Office Action argues that *Gaytan* discloses "storing a first subset of packet data..." (OA page 4, line 20). Applicants respectfully disagree. More specifically *Gaytan* discloses:

> upon detecting that the word packing circuit is ready to transmit data, a byte rotate circuit within the byte packing circuit calculates a select value configuring the appropriate data path between the input, save and output storage elements 660, 665 and 670. This data path is used to effectively add bytes of data from one word to another to "byte pack" the output data packet transferred to the TX buffer memory (Step 120).... Finally, in Step 130, a determination is made as to whether the transfer of the first sequence of data words completes the data transfer of the data block before transferring any remaining bytes in the output storage element to the TX buffer memory. If so, the data transfer is complete. Otherwise, the word and byte packing circuits continue its packing operations on a subsequent data blocks associated with other TX data buffers.

(Emphasis added).

As illustrated in this passage, *Gaytan* appears to disclose that all of the data is sent to the TX buffer memory, where, as recited in claim 1, a second subset of data is stored "***in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word***." *Gaytan* fails to even suggest an alignment register, not to mention storing data in an alignment register upon fulfillment of a condition.

Additionally, *Priem* fails to overcome the deficiencies of *Gaytan*. For at least these reasons, claim 1 is allowable.

B. Claim 5 is Allowable Over *Priem* in view of *Gaytan*

The Office Action indicates that claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Number 6,282,587 ("*Priem*") in view of U.S. Patent Number 5,638,367 ("*Gaytan*"). Applicants respectfully traverse this rejection for at least the reason that *Priem* in view of *Gaytan* fails to disclose, teach, or suggest all of the elements of claim 5. More specifically, claim 5 recites:

> A system for transferring network packet data stored in memory to an output device, the system comprising:
> a direct memory access (DMA) interface for accessing a set of data words stored in memory, each data word having at least one valid octet to be included in a network packet and each data word being accessed using a DMA address associated with the data word;
> a first in-first out (FIFO) buffer for storing network packet data to be transmitted by the output device; and
> an alignment block having at least one alignment register, wherein the alignment register for storing at least one data octet, and wherein the alignment block is adapted to:
> concatenate one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet ***to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word***;
> store the first sequence of packet data octets in a FIFO buffer operably connected to the output device ***when the octet length of the sequence of packet data octets is equal to the octet length of a data word***; and
> store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence ***in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word***.
> ***(Emphasis added).***

Applicants respectfully submit that claim 5 is allowable over the cited art for at least the reason that neither *Priem* nor *Gaytan*, taken alone or in combination, discloses, teaches, or suggests a "system for transferring network packet data stored in memory to an output device, the system comprising… an alignment block… adapted to… concatenate one or more packet data octets from at least a first data word having at least one packet data octet to be included in

a network packet ***to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word***... store the first sequence of packet data octets in a FIFO buffer operably connected to the output device ***when the octet length of the sequence of packet data octets is equal to the octet length of a data word***... [and] store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence ***in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word***" as recited in claim 5.

First, the Office Action argues that *Gaytan* discloses "concatenating the first sequence..." (OA page 4, line 13). Applicants respectfully disagree. More specifically, *Gaytan* discloses "perform[ing] packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry; namely, a word packing circuit and a byte packing circuit. Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 54). As illustrated in this passage, *Gaytan* appears to disclose packing operations but fails to disclose anything related to "concatenating one or more packet data octets... ***to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word***" as recited in claim 5.

Second, the Office Action argues that *Gaytan* discloses "storing a first sequence of packet data octets when the octet length of the sequence of data" (OA page 4, line 17). Applicants respectfully disagree. More specifically, *Gaytan* discloses "perform[ing] packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry; namely, a word packing circuit and a byte packing circuit. Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 54). As illustrated in this passage, *Gaytan* appears to disclose always storing data in the TX buffer. Consequently, *Gaytan* fails to even suggest "storing the first sequence of packet data octets in a

FIFO buffer... ***when the octet length of the sequence of packet data octets is equal to the octet length of a data word***" as recited in claim 5. Further, *Gaytan* does not even appear to suggest making a determination of octet length, as implicitly recited in this element of claim 5.

Third, the Office Action argues that *Gaytan* discloses "storing a first subset of packet data..." (OA page 4, line 20). Applicants respectfully disagree. More specifically *Gaytan* discloses:

> upon detecting that the word packing circuit is ready to transmit data, a byte rotate circuit within the byte packing circuit calculates a select value configuring the appropriate data path between the input, save and output storage elements 660, 665 and 670. This data path is used to effectively add bytes of data from one word to another to "byte pack" the output data packet transferred to the TX buffer memory (Step 120).... Finally, in Step 130, a determination is made as to whether the transfer of the first sequence of data words completes the data transfer of the data block before transferring any remaining bytes in the output storage element to the TX buffer memory. If so, the data transfer is complete. Otherwise, the word and byte packing circuits continue its packing operations on a subsequent data blocks associated with other TX data buffers.

(Emphasis added).

As illustrated in this passage, *Gaytan* appears to disclose that all of the data is sent to the TX buffer memory, where, as recited in claim 5, a second subset of data is stored "***in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word***." *Gaytan* fails to even suggest an alignment register, not to mention storing data in an alignment register upon fulfillment of a condition, claim 5 is allowable.

Additionally, *Priem* fails to overcome the deficiencies of *Gaytan*. For at least these reasons, claim 5 is allowable.

C. Claims 2 – 4 and 6 – 13 are Allowable Over *Priem* in view of *Gaytan*

The Office Action indicates that claims 2 – 4 and 6 – 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Number 6,282,587 ("*Priem*") in view of U.S. Patent Number 5,638,367 ("*Gaytan*"). Applicants respectfully traverse this rejection for at least the reason that *Priem* in view of *Gaytan* fails to disclose, teach, or suggest all of the elements of claim 2 – 4 and 6 – 13. More specifically, dependent claims 2 – 4 are believed to be allowable for at least the reason that these claims depend from allowable independent claim 1. Dependent claims 6 – 13 are believed to be allowable for at least the reason that they depend from allowable independent claim 5. *In re Fine*, *Minnesota Mining and Mfg.Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002).

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested.

Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and Official Notice, or statements interpreted similarly, should not be considered well-known for the particular and specific reasons that the claimed combinations are too complex to support such conclusions and because the Office Action does not include specific findings predicated on sound technical and scientific reasoning to support such conclusions.

If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

/afb/
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